STD100N3LF3

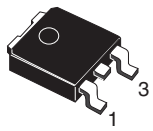
N-channel 30 V, 0.0045 Ω, 80 A, DPAK planar STripFET™ II Power MOSFET

Features

Type	V_{DSSS}	$R_{DS(on)}$	I_D	Pw
STD100N3LF3	30 V	<0.0055 Ω	80 A(1)	110 W

1. Current limited by package

- 100% avalanche tested
- Logic level threshold



DPAK

Applications

- Switching application
  - Automotive

Description

This STripFET™ II Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

Figure 1. Internal schematic diagram

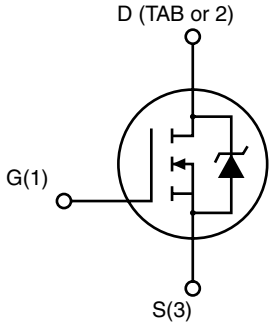


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD100N3LF3	100N3LF3	DPAK	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C=100 °C	70	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
	Derating factor	0.73	W/°C
dv/dt (3)	Peak diode recovery voltage slope	3.9	V/ns
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Max. operating junction temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80A$, di/dt $\leq$360 A/µs, $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	1.36	°C/W
R_{thJA}	Thermal resistance junction-ambient max	100	°C/W
T_l	Maximum lead temperature for soldering purpose	275	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Not-repetitive avalanche current (pulse width limited by T_J max)	40	A
E_{AS}	Single pulsed avalanche energy (starting T_J = 25 °C, $I_D = I_{AV}$, V_{DD} = 24 V)	500	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 40 A V_{GS} = 5 V, I_D = 20 A		0.0045 0.008	0.0055 0.01	Ω Ω
		V_{GS} = 10 V, I_D = 40 A @125 °C V_{GS} = 5 V, I_D = 20 A @125 °C		0.0068 0.0146		Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V, I_D = 15 A	-	31		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2060 728 67		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 24 V, I_D = 80 A V_{GS} = 5 V	-	20 7 7.5	27	nC nC nC
R_G	Gate input resistance	f = 1 MHz gate DC Bias = 0 test signal level = 20 mV open drain	-	1.9		Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 15 V, I_D= 40 A,	-	9	-	ns
t_r	Rise time	R_G=4.7Ω, V_{GS}=10 V		205		ns
$t_{d(off)}$	Turn-off delay time			31		ns
t_f	Fall time			35		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM}(1)	Source-drain current (pulsed)		-		320	A
V_{SD}(2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A,	-	40		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,		40		µC
I_{RRM}	Reverse recovery current	V_{DD} = 25 V, T_J = 150 °C		2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

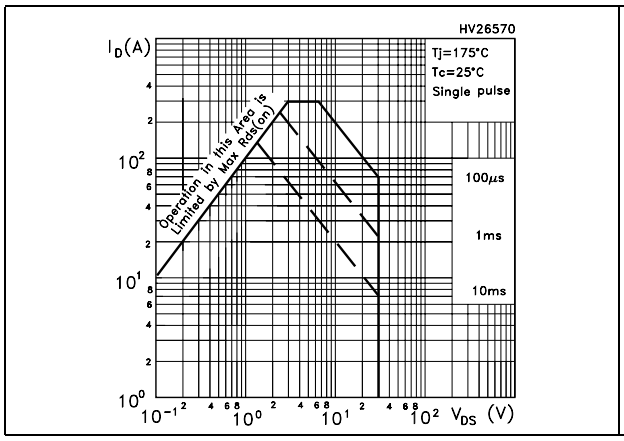


Figure 3. Thermal impedance

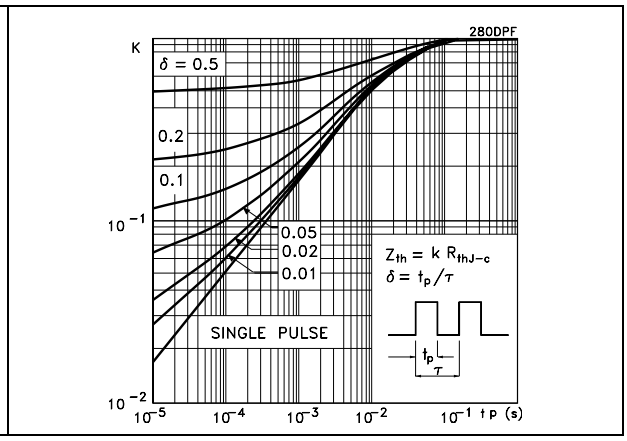


Figure 4. Output characteristics

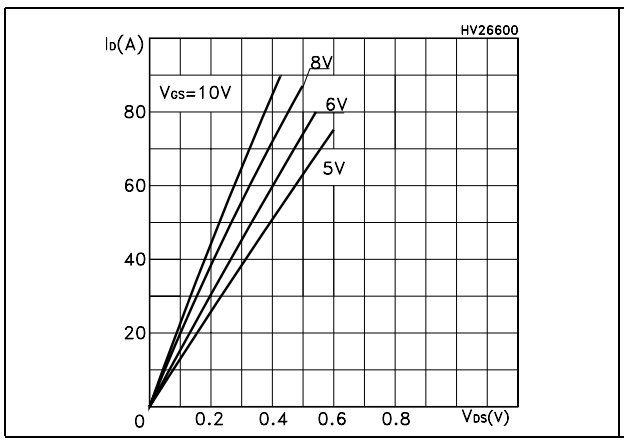


Figure 5. Transfer characteristics

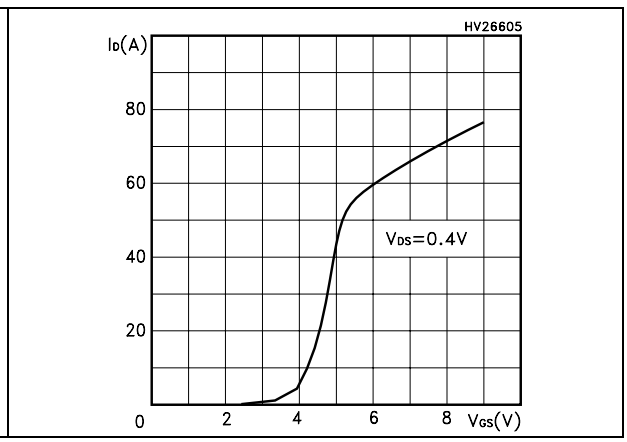


Figure 6. Transconductance

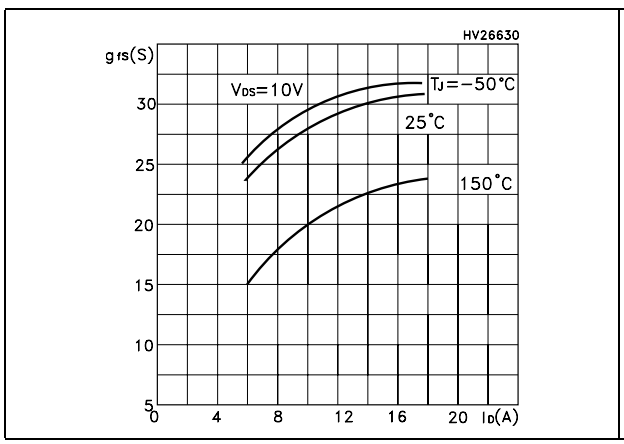


Figure 7. Static drain-source on resistance