NCE P-Channel Enhancement Mode Power MOSFET
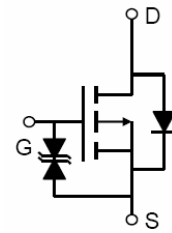
Description

The NCE01P13K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

General Features

● V_{DS} =-100V,I_D =-13A

$R_{DS(ON)}$ <200mΩ @ V_{GS}=-10V   (Typ:170mΩ)

● Super high dense cell design
● Advanced trench process technology
● Reliable and rugged
● High density celldesign for ultra low on-resistance
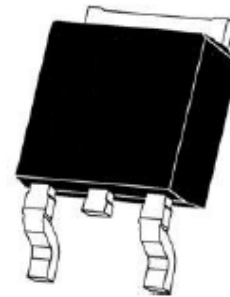
Application

● Power switch
● DC/DC converters

Schematic diagram

Marking and pin assignment

TO-252 -2Ltop view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE01P13K	NCE01P13K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-13	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-9.2	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	40	W
Derating factor		0.32	W/℃
Single pulse avalanche energy [Note 5]	E_{AS}	110	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta Jc}$	3.13	℃/W

Electrical Characteristics (T$_C$=25℃ unless otherwise noted)

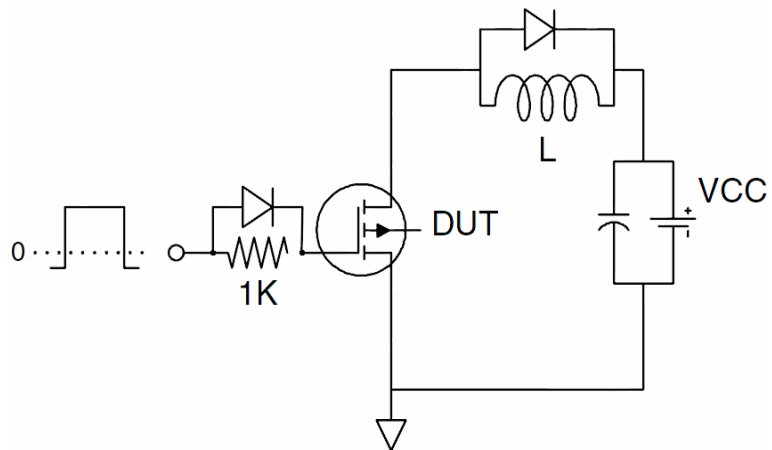| Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV$_{DSS}$	V$_{GS}$=0V I$_D$=-250µA	-100	-	-	V
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$=-100V,V$_{GS}$=0V	-	-	1	µA
Gate-Body Leakage Current	I$_{GSS}$	V$_{GS}$=±20V,V$_{DS}$=0V	-	-	±10	µA
On Characteristics [Note 3]						
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$=V$_{GS}$,I$_D$=-250µA	-1	-1.9	-3	V
Drain-Source On-State Resistance	R$_{DS(ON)}$	V$_{GS}$=-10V, I$_D$=-16A	-	170	200	mΩ
Forward Transconductance	g$_{FS}$	V$_{DS}$=-15V,I$_D$=-5A	12	-	-	S
Dynamic Characteristics [Note4]						
Input Capacitance	C$_{Iss}$	V$_{DS}$=-25V,V$_{GS}$=0V, F=1.0MHz	-	760	-	PF
Output Capacitance	C$_{oss}$		-	260	-	PF
Reverse Transfer Capacitance	C$_{rss}$		-	170	-	PF
Switching Characteristics [Note 4]						
Turn-on Delay Time	t$_{d(on)}$	V$_{DD}$=-50V,I$_D$=-10A V$_{GS}$=-10V,R$_{GEN}$=9.1Ω	-	14	-	nS
Turn-on Rise Time	t$_r$		-	18	-	nS
Turn-Off Delay Time	t$_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t$_f$		-	18	-	nS
Total Gate Charge	Q$_g$	V$_{DS}$=-50V,I$_D$=-10A, V$_{GS}$=-10V	-	25	-	nC
Gate-Source Charge	Q$_{gs}$		-	5	-	nC
Gate-Drain Charge	Q$_{gd}$		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [Note 3]	V$_{SD}$	V$_{GS}$=0V,I$_S$=-10A	-	-	-1.2	V
Diode Forward Current [Note 2]	I$_S$	-	-	-	-13	A
Reverse Recovery Time	t$_{rr}$	TJ = 25°C, IF =-10A di/dt = 100A/µs[Note3]	-	35	-	nS
Reverse Recovery Charge	Qrr		-	46	-	nC
Forward Turn-On Time	t$_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. E$_{AS}$ condition：Tj=25℃,V$_{DD}$=-50V,V$_G$=-10V,L=0.5mH,Rg=25Ω
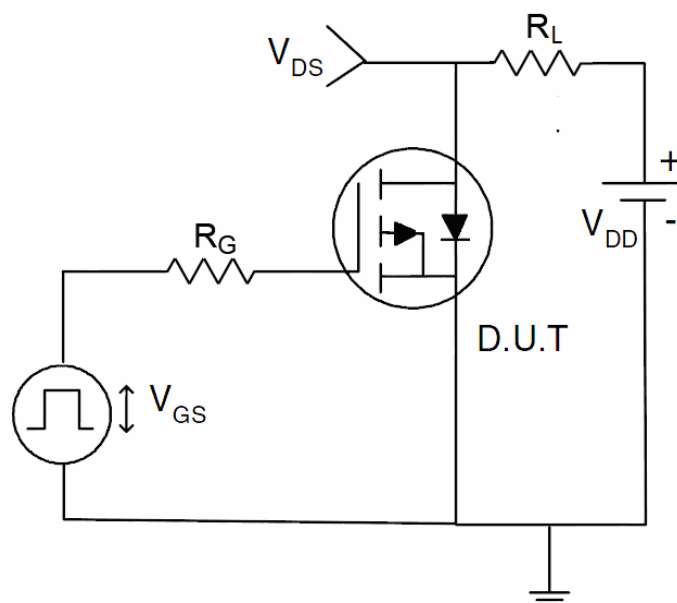
Test Circuit

1) E$_{AS}$ Test Circuit

2) Gate Charge Test Circuit

3) Switch Time Test Circuit

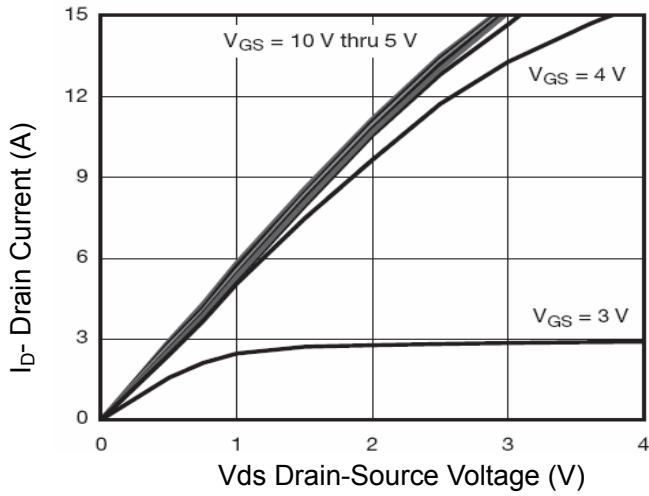## Typical Electrical and Thermal Characteristics (Curves)
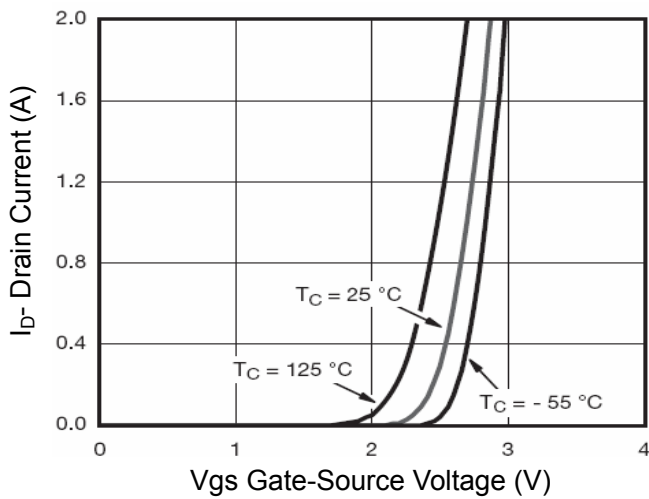
Figure 1 Output Characteristics
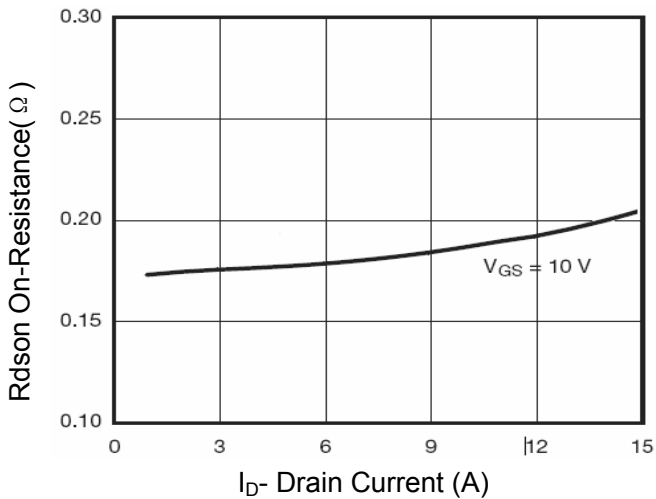
Figure 2 Transfer Characteristics

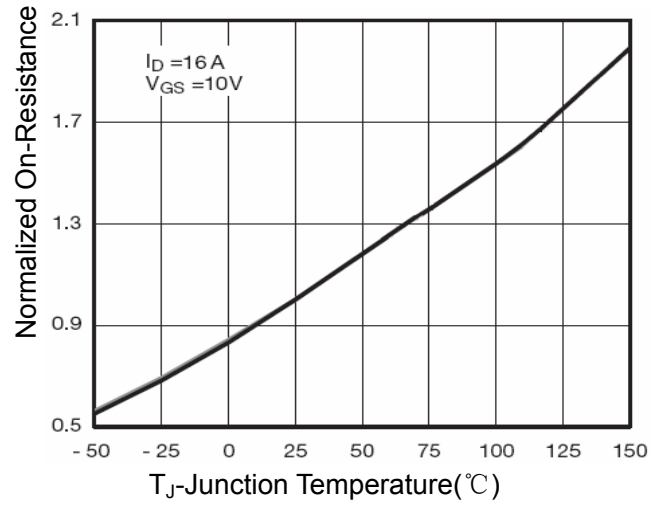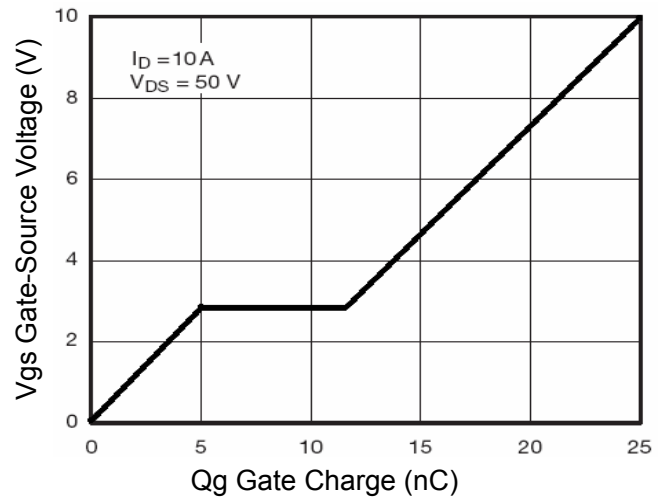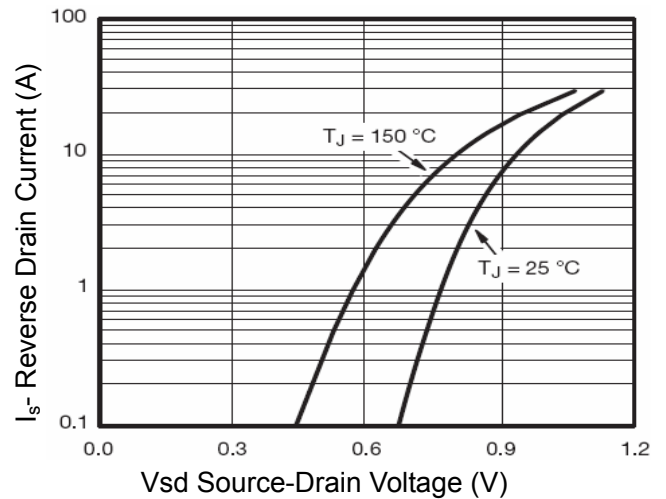**Figure 3 Rdson- Drain Current**

Figure 4 Rdson-JunctionTemperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward