ISL9N308AD3 / ISL9N308AD3ST

N-Channel Logic Level UltraFET® Trench Power MOSFETs 30V, 50A, 8mΩ

General Description

This device employs a new advanced trench MOSFET technology and features low gate charge while maintaining low on-resistance.

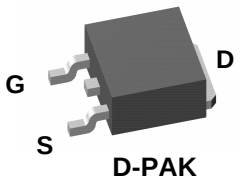
Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

Applications

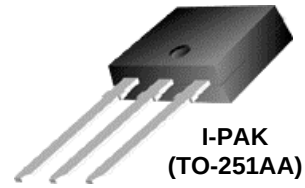
- DC/DC converters

Features

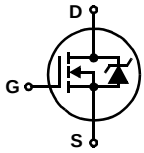
- Fast switching
- $r_{DS(ON)}$ = 0.0064Ω (Typ), V_{GS} = 10V
- $r_{DS(ON)}$ = 0.010Ω (Typ), V_{GS} = 4.5V
- Q_g (Typ) = 24nC, V_{GS} = 5V
- Q_{gd} (Typ) = 8nC
- C_{ISS} (Typ) = 2600pF



D-PAK
(TO-252)



I-PAK
(TO-251AA)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10V) Note 1	50	A
	Continuous (T_C = 100°C, V_{GS} = 4.5V) Note 1	48	A
	Continuous (T_C = 25°C, V_{GS} = 10V, $R_{\theta JC}$ = 52°C/W)	14	A
	Pulsed	Figure 4	A
P_D	Power dissipation Derate above 25°C	100 0.67	W W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
N308AD	ISL9N308AD3ST	TO-252AA	330mm	16mm	2500 units
N308AD	ISL9N308AD3	TO-251AA	Tube	N/A	75 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25V	-	-	1	μA
		V_{GS} = 0V, T_C = 150°	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 50A, V_{GS} = 10V	-	0.0064	0.008	Ω
		I_D = 48A, V_{GS} = 4.5V	-	0.010	0.012	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	2600	-	pF
C_{OSS}	Output Capacitance		-	520	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	225	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 48A, I_g = 1.0mA	-	45	68	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V	-	24	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V	-	2.6	4.0	nC
Q_{gs}	Gate to Source Gate Charge		-	7	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	8	-	nC
Switching Characteristics (V_{GS} = 4.5V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 14A, V_{GS} = 4.5V, R_{GS} = 6.2Ω	-	-	122	ns
$t_{d(ON)}$	Turn-On Delay Time		-	15	-	ns
t_r	Rise Time		-	67	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	35	-	ns
t_f	Fall Time		-	32	-	ns
t_{OFF}	Turn-Off Time		-	-	100	ns
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 14A, V_{GS} = 10V, R_{GS} = 6.2Ω	-	-	71	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	40	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	64	-	ns
t_f	Fall Time		-	31	-	ns
t_{OFF}	Turn-Off Time		-	-	142	ns
Unclamped Inductive Switching						
t_{AV}	Avalanche Time	I_D = 3.2A, L = 3.0mH	215	-	-	μs
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 48A	-	-	1.25	V
		I_{SD} = 20A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 48A, dI_{SD}/dt = 100A/μs	-	-	26	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 48A, dI_{SD}/dt = 100A/μs	-	-	14	nC

Notes:
1: TO-251AA continuous current limited by package to 35A.

Typical Characteristic T_C = 25°C unless otherwise noted

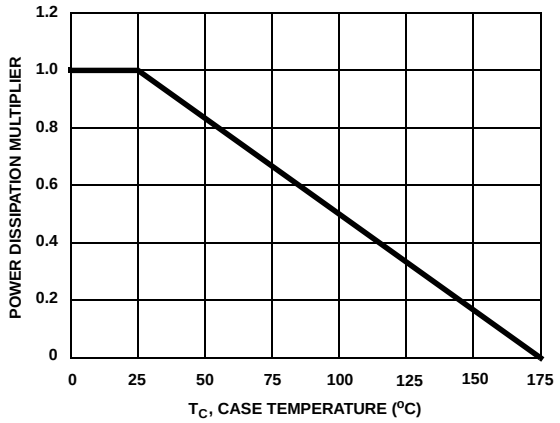


Figure 1. Normalized Power Dissipation vs Ambient Temperature

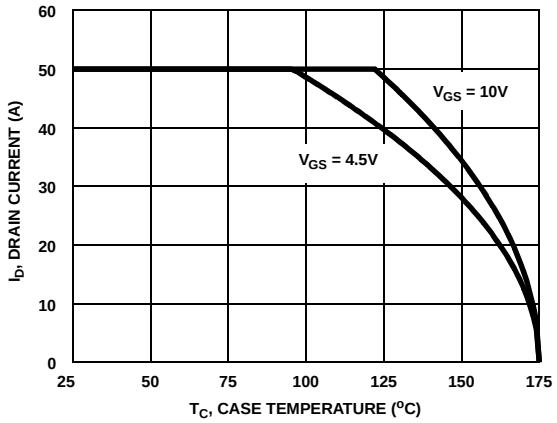


Figure 2. Maximum Continuous Drain Current vs Case Temperature

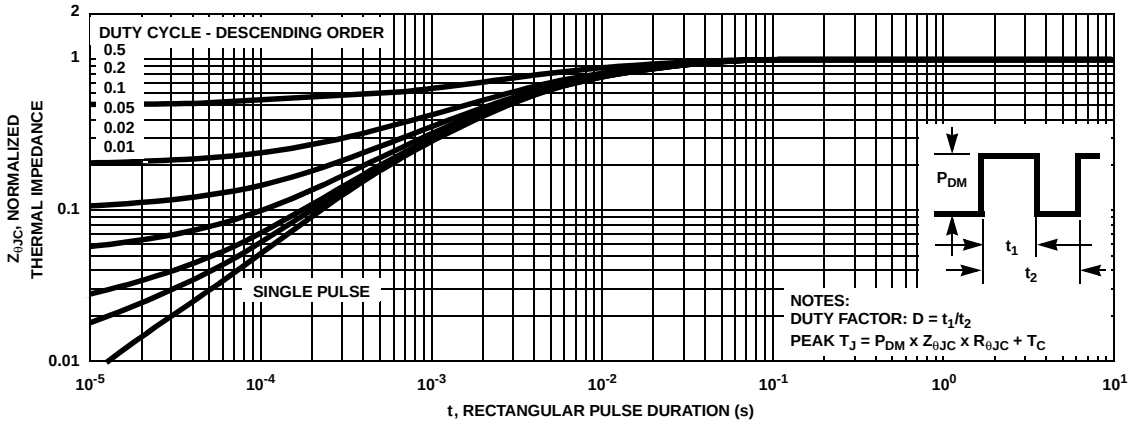


Figure 3. Normalized Maximum Transient Thermal Impedance

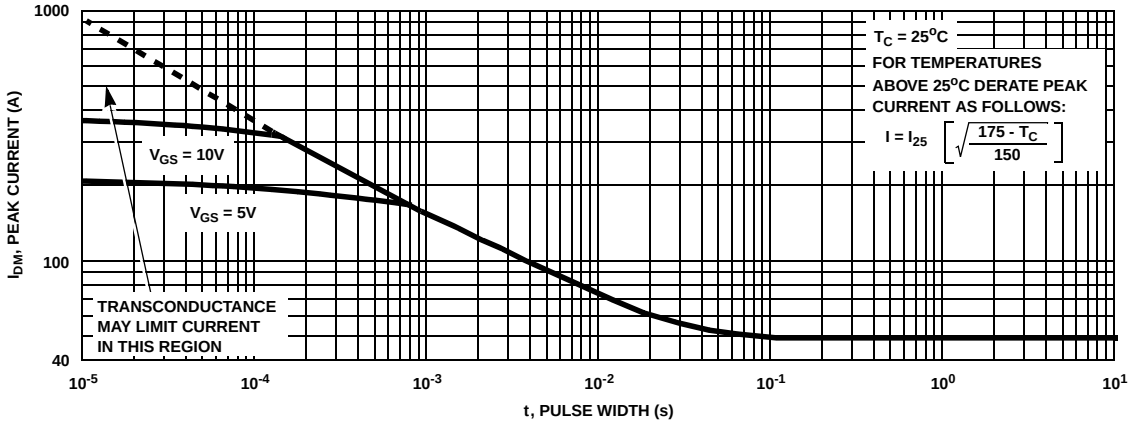


Figure 4. Peak Current Capability