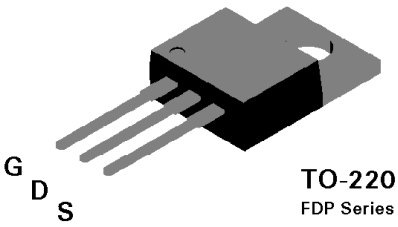
FDP603AL / FDB603AL
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

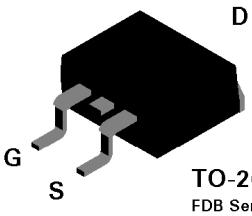
These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

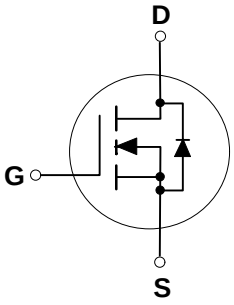
- 33 A, 30 V. $R_{DS(ON)}$ = 0.022 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$ = 0.036 Ω @ V_{GS}=4.5 V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low $R_{DS(ON)}$.
- 175°C maximum junction temperature rating.



TO-220
FDP Series



TO-263AB
FDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP603AL	FDB603AL	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
I_D	Drain Current - Continuous	33		A
	- Pulsed (Note 1)	100		
P_D	Total Power Dissipation @ T_C = 25°C	50		W
	Derate above 25°C	0.33		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 12 A			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				12	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		32		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.8	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 °C		-4.5		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 25 A		0.018	0.022	Ω
		T_J =125 °C		0.026	0.035	
		V_{GS} = 4.5 V, I_D = 10 A		0.03	0.036	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 25 A		24		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		670		pF
C_{oss}	Output Capacitance			345		pF
C_{rss}	Reverse Transfer Capacitance			95		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 25 A		8	16	nS
t_r	Turn - On Rise Time	V_{GS} = 10 V, R_{GEN} = 24 Ω		102	140	nS
$t_{D(off)}$	Turn - Off Delay Time			20	36	nS
t_f	Turn - Off Fall Time			80	115	nS
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 25 A, V_{GS} = 10 V		19	26	nC
Q_{gs}	Gate-Source Charge			3.5		nC
Q_{gd}	Gate-Drain Charge			5.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				25	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 25 A (Note 1)		1	1.3	V
		T_J = 125°C		0.85	1.1	

Note
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

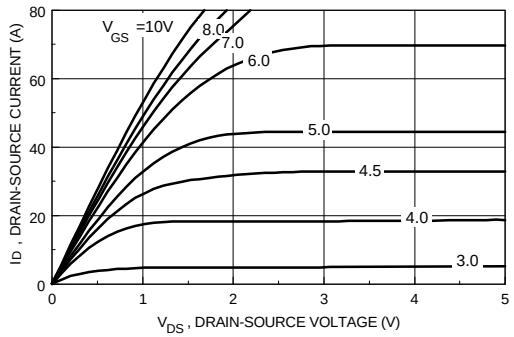


Figure 1. On-Region Characteristics.

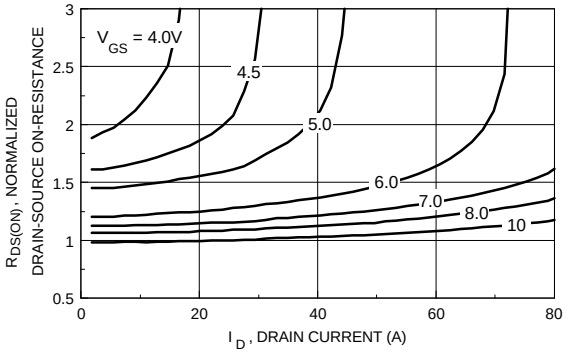


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

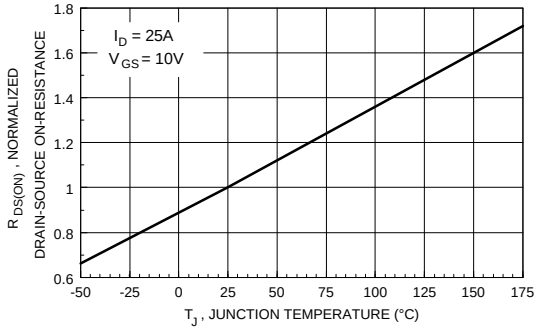


Figure 3. On-Resistance Variation with Temperature.

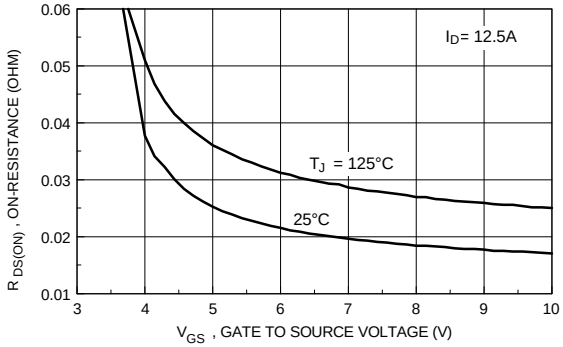


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

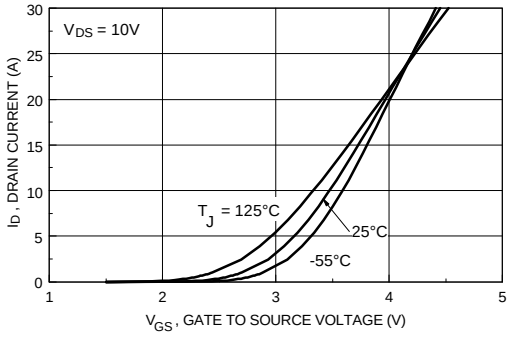


Figure 5. Transfer Characteristics.

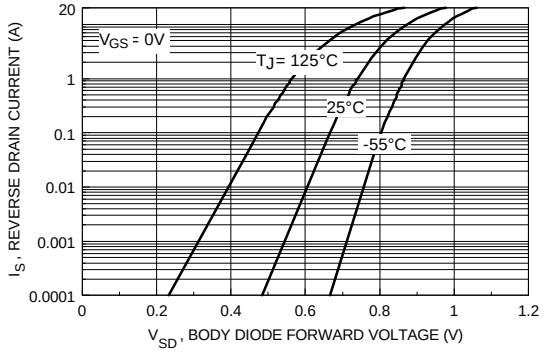


Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.