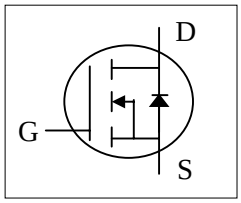
AP9465BGH/J

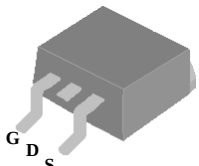
Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

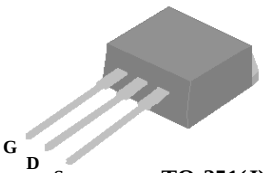
- ▼ **Lower Gate Charge**
- ▼ **Simple Drive Requirement**
- ▼ **Fast Switching Characteristic**



BV_{DSS}	40V
$R_{DS(ON)}$	32mΩ
I_D	20A



TO-252(H)



TO-251(J)

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications. The through-hole version (AP9465BGJ) are available for low-profile applications.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current	20	A
I_D@T_C=100℃	Continuous Drain Current	12	A
I_{DM}	Pulsed Drain Current[1]	60	A
P_D@T_C=25℃	Total Power Dissipation	20.8	W
	Linear Derating Factor	0.17	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	6.0	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount)[3]	62.5	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	110	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=12A	-	-	32	mΩ
		V_{GS}=4.5V, I_D=8A	-	-	45	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=12A	-	15	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=40V, V_{GS}=0V	-	-	10	uA
	Drain-Source Leakage Current (T_j=125°C)	V_{DS}=32V, V_{GS}=0V	-	-	250	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=12A	-	6.6	11	nC
Q_{gs}	Gate-Source Charge	V_{DS}=32V	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=20V	-	4.7	-	ns
t_r	Rise Time	I_D=12A	-	23	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	16	-	ns
t_f	Fall Time	R_D=1.67Ω	-	3	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	450	720	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	70	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=12A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=12A, V_{GS}=0V,	-	19	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	11	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board

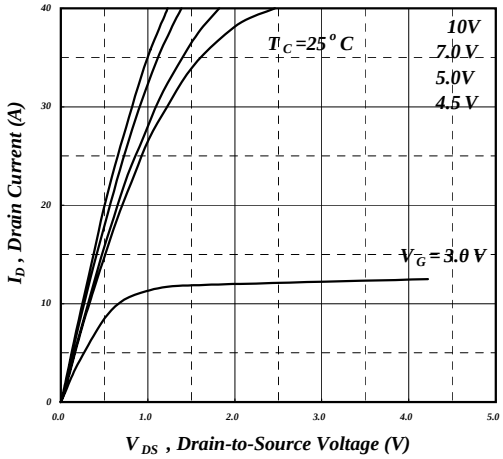


Fig 1. Typical Output Characteristics

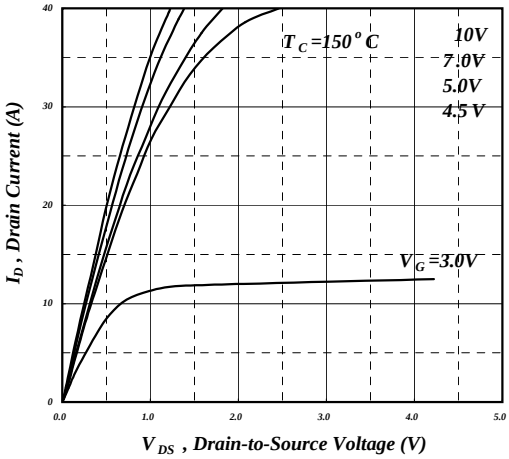


Fig 2. Typical Output Characteristics

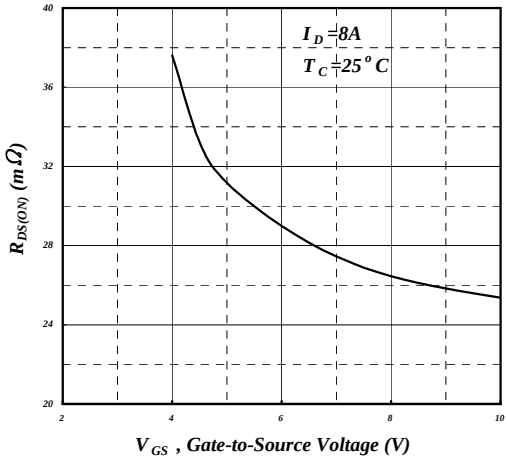


Fig 3. On-Resistance v.s. Gate Voltage

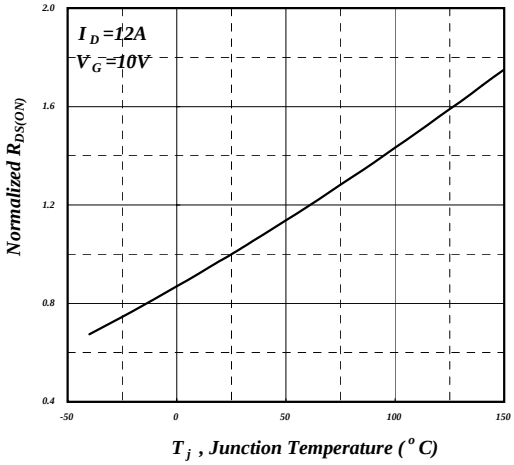


Fig 4. Normalized On-Resistance v.s. Junction Temperature

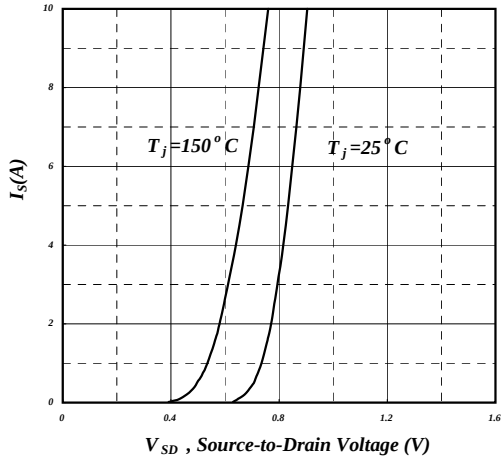


Fig 5. Forward Characteristic of Reverse Diode

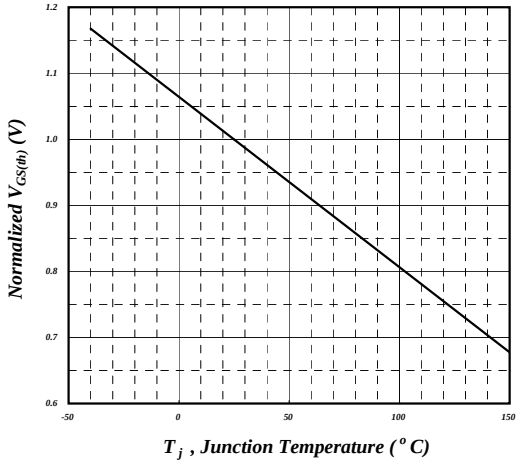


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

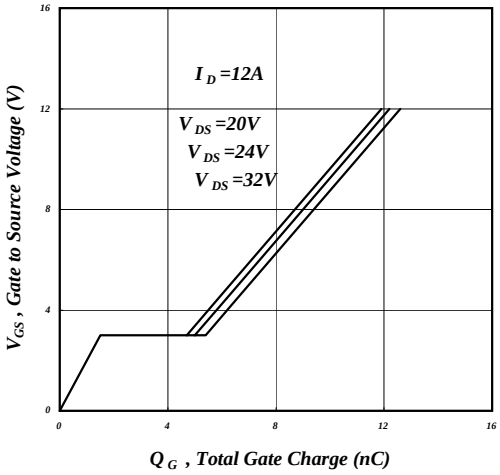


Fig 7. Gate Charge Characteristics

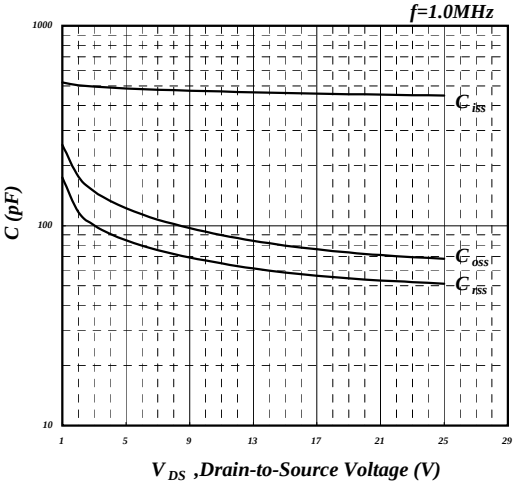


Fig 8. Typical Capacitance Characteristics

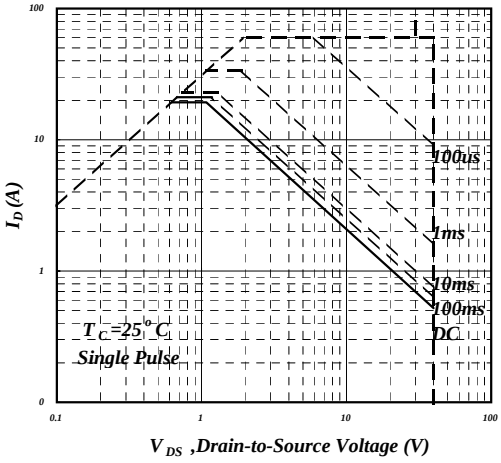


Fig 9. Maximum Safe Operating Area

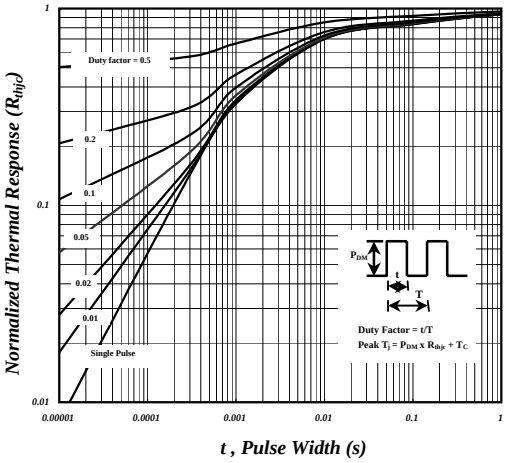


Fig 10. Effective Transient Thermal Impedance

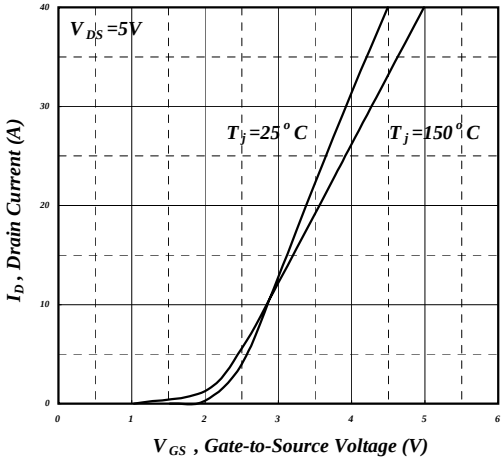


Fig 11. Transfer Characteristics

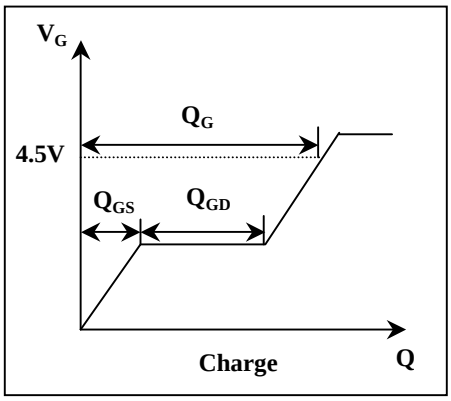


Fig 12. Gate Charge Waveform