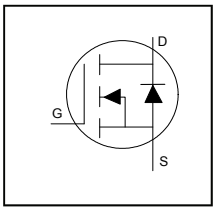
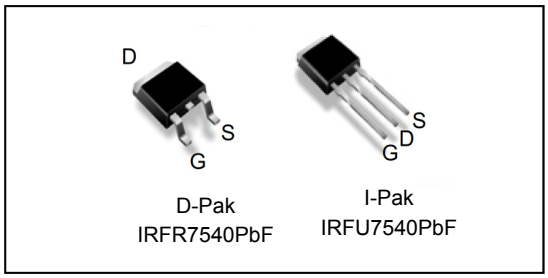
Application
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}	60V
$R_{DS(on)}$ typ.	4.0mΩ
max	4.8mΩ
I_D (Silicon Limited)	110A①
I_D (Package Limited)	90A



G	D	S
Gate	Drain	Source

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFR7540PbF	D-Pak	Tube	75	IRFR7540PbF
		Tape and Reel	2000	IRFR7540TRPbF
		Tape and Reel Left	3000	IRFR7540TRLPbF
IRFU7540PbF	I-Pak	Tube	75	IRFU7540PbF

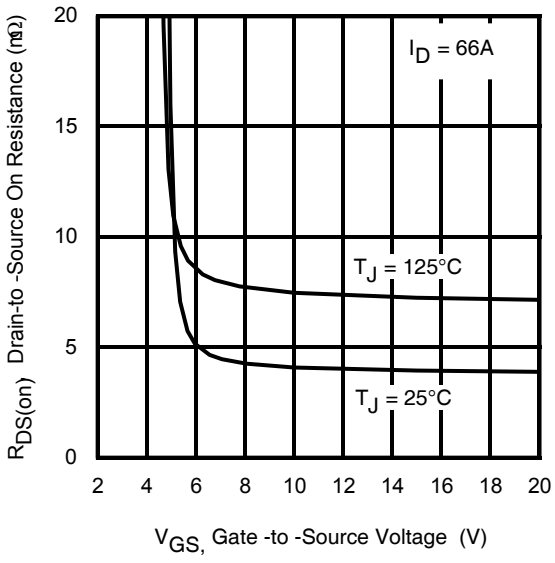


Fig 1. Typical On-Resistance vs. Gate Voltage

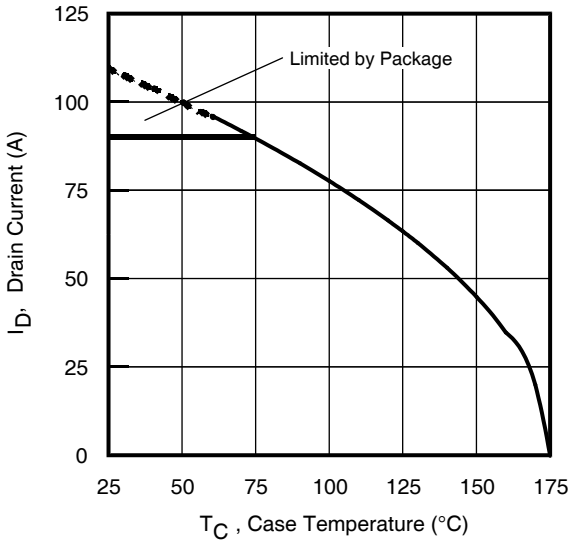


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	110①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	78	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	90	
I_{DM}	Pulsed Drain Current ②	440*	
P_D @T_C = 25°C	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	160	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑩	273	
I_{AR}	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑨	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

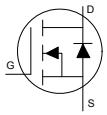
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	48	——	mV/°C	Reference to 25°C, I_D = 1mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.0	4.8	mΩ	V_{GS} = 10V, I_D = 66A
		——	5.2	——		V_{GS} = 6.0V, I_D = 33A
$V_{GS(th)}$	Gate Threshold Voltage	2.1	——	3.7	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 60V, V_{GS} = 0V
		——	——	150		V_{DS} = 60V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	2.4	——	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	200	——	——	S	V_{DS} = 10V, I_D =66A
Q_g	Total Gate Charge	——	86	130	nC	I_D = 66A
Q_{gs}	Gate-to-Source Charge	——	22	——		V_{DS} = 30V
Q_{gd}	Gate-to-Drain Charge	——	27	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg– Qgd)	——	59	——		
$t_{d(on)}$	Turn-On Delay Time	——	8.7	——	ns	V_{DD} = 30V
t_r	Rise Time	——	38	——		I_D = 66A
$t_{d(off)}$	Turn-Off Delay Time	——	59	——		R_G= 2.7Ω
t_f	Fall Time	——	32	——		V_{GS} = 10V⑤
C_{iss}	Input Capacitance	——	4360	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	410	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	260	——		f = 1.0MHz, See Fig.7
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	410	——		V_{GS} = 0V, VDS = 0V to 48V⑦
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	——	530	——		V_{GS} = 0V, VDS = 0V to 48V⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	110①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	440*		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J = 25°C,I_S = 66A,V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery dv/dt④	——	11	——	V/ns	T_J = 175°C,I_S = 66A,V_{DS} = 60V
t_{rr}	Reverse Recovery Time	——	34	——	ns	T_J = 25°C V_{DD} = 51V
		——	37	——		T_J = 125°C I_F = 66A,
Q_{rr}	Reverse Recovery Charge	——	36	——	nC	T_J = 25°C di/dt = 100A/μs ⑤
		——	47	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	1.9	——	A	T_J = 25°C

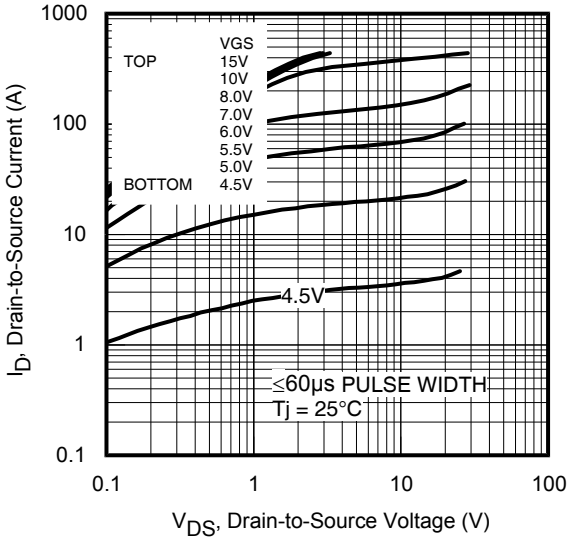


Fig 3. Typical Output Characteristics

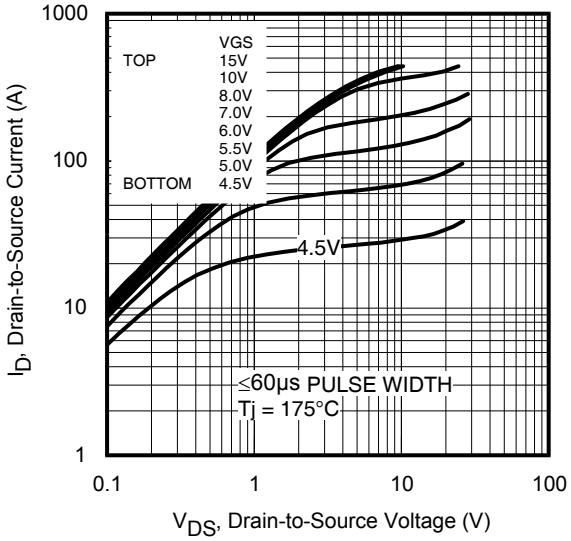


Fig 4. Typical Output Characteristics

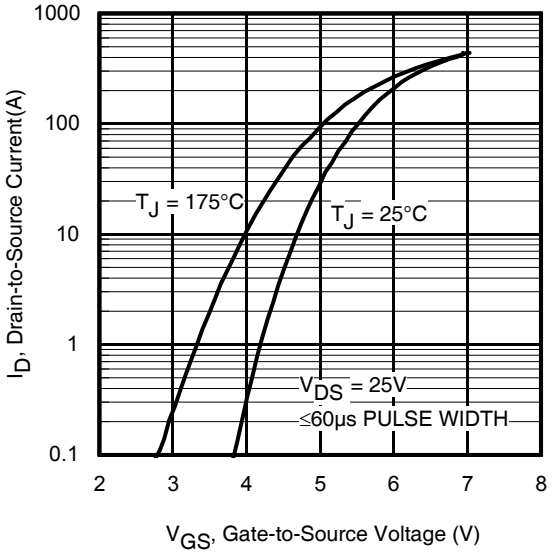


Fig 5. Typical Transfer Characteristics

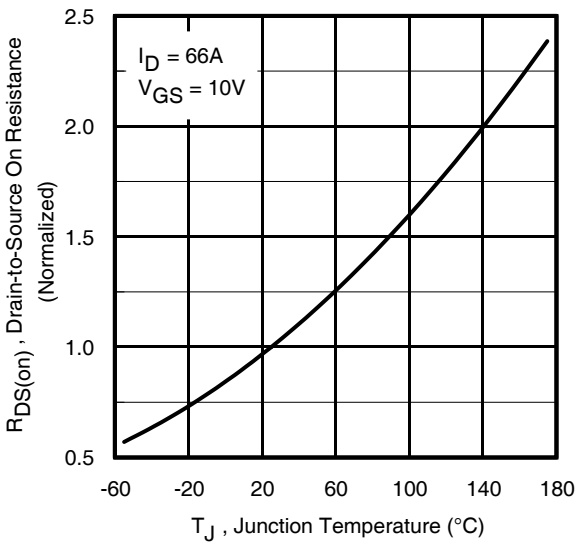


Fig 6. Normalized On-Resistance vs. Temperature

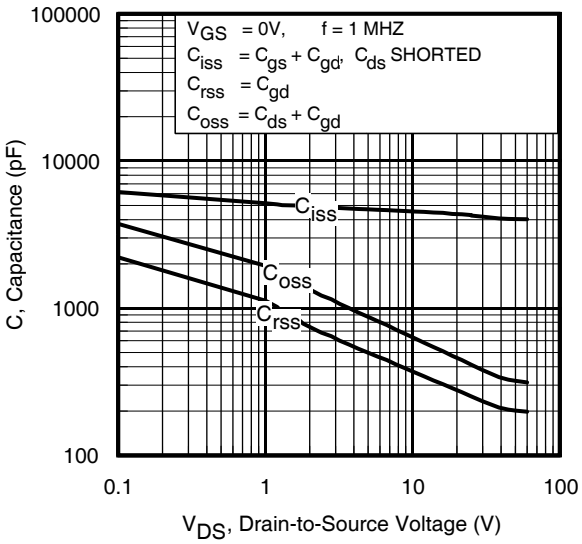


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

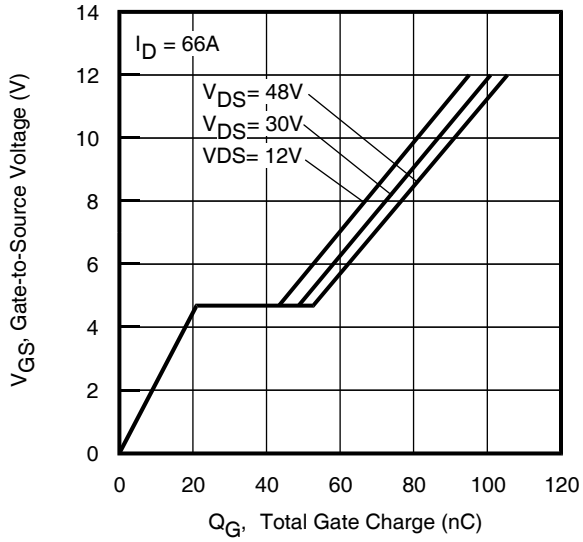


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

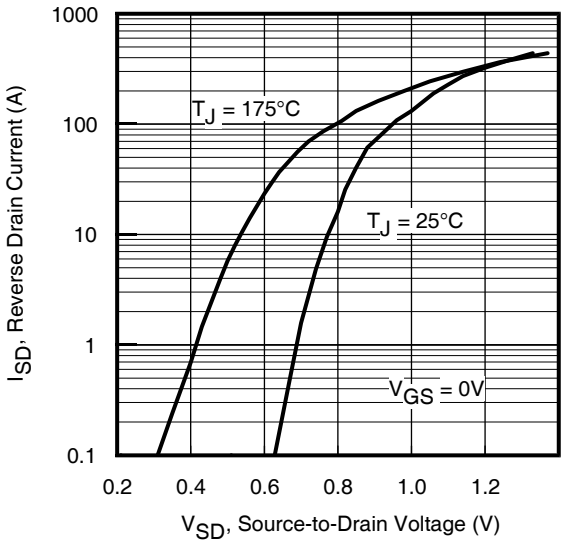


Fig 9. Typical Source-Drain Diode Forward Voltage

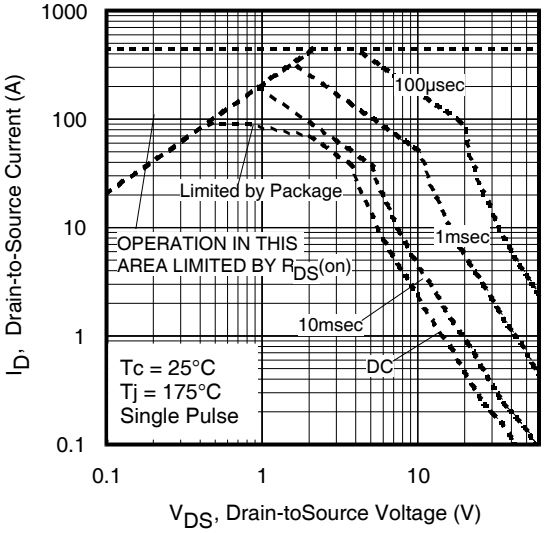


Fig 10. Maximum Safe Operating Area

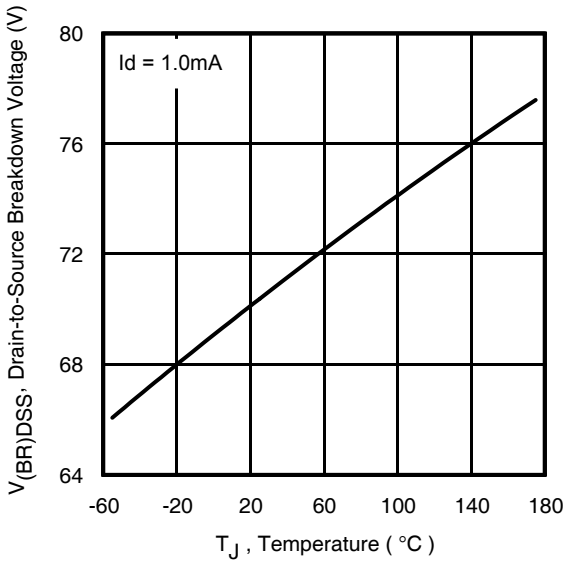


Fig 11. Drain-to-Source Breakdown Voltage

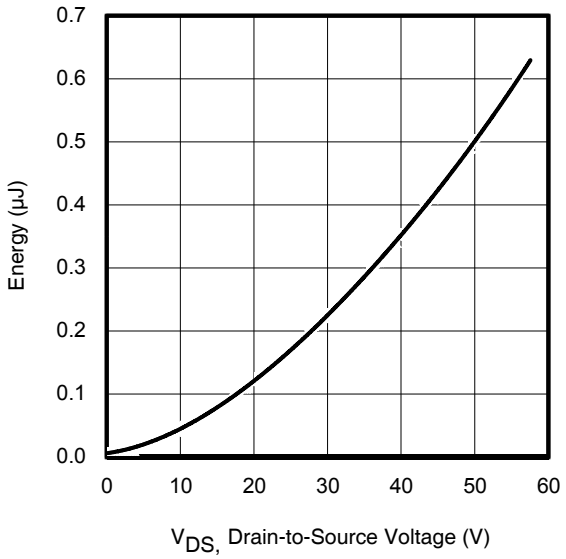


Fig 12. Typical C_{oss} Stored Energy

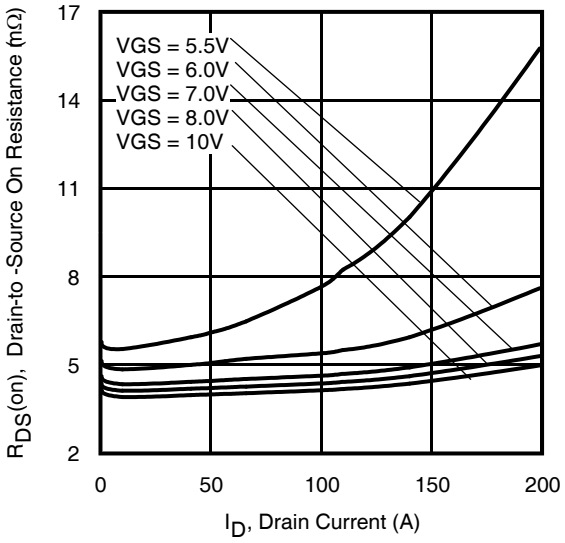


Fig 13. Typical On-Resistance vs. Drain Current

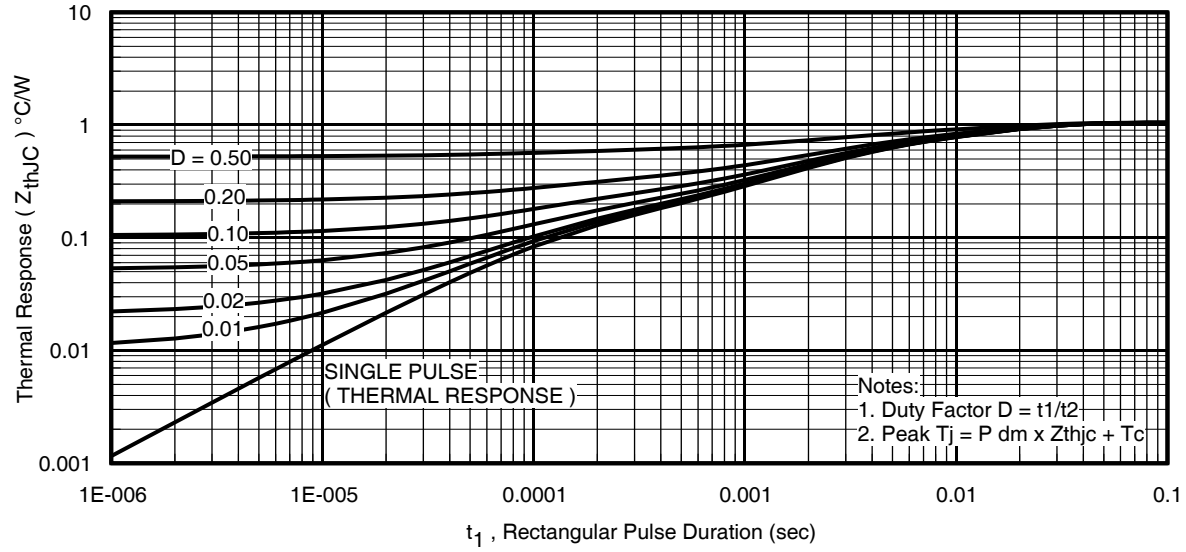


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

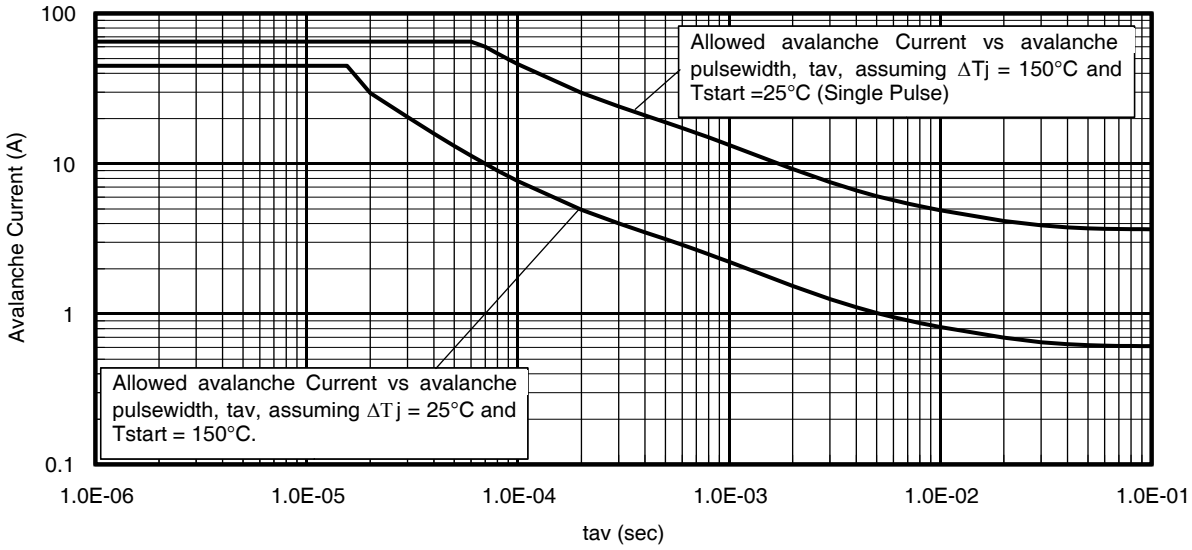


Fig 15. Avalanche Current vs. Pulse Width

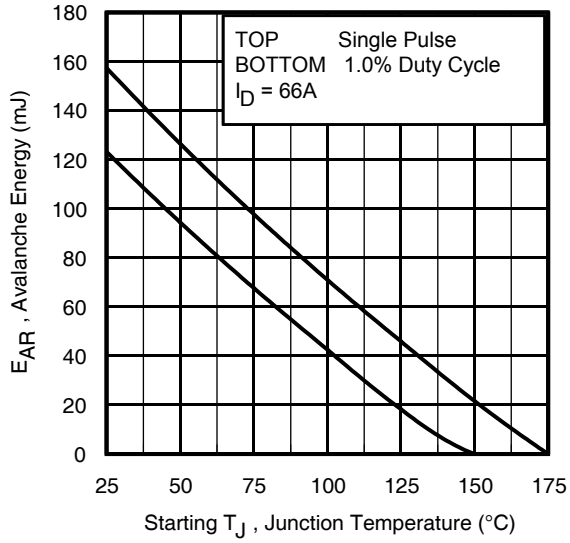


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

PD (ave) = 1/2 (1.3·BV·I_{av}) = ΔT/ Z_{thJC}

I_{av} = 2ΔT/ [1.3·BV·Z_{th}]

$E_{AS\ (AR)}$ = $P_{D\ (ave)}$·t_{av}

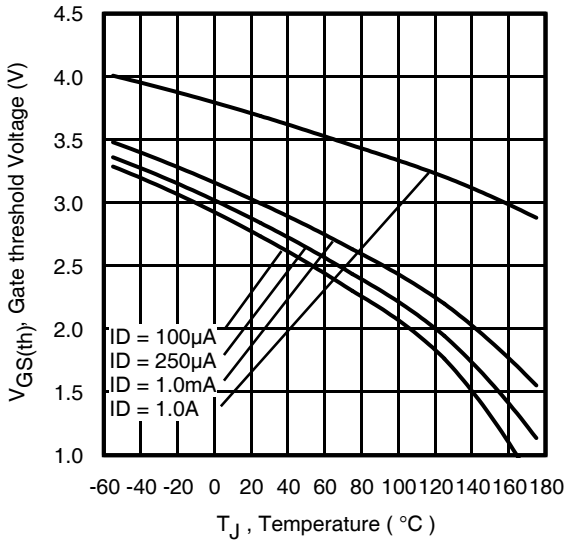


Fig 17. Threshold Voltage vs. Temperature

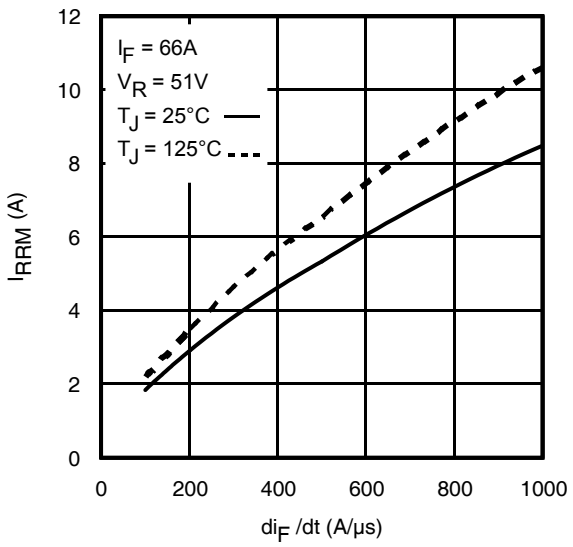


Fig 18. Typical Recovery Current vs. dif/dt

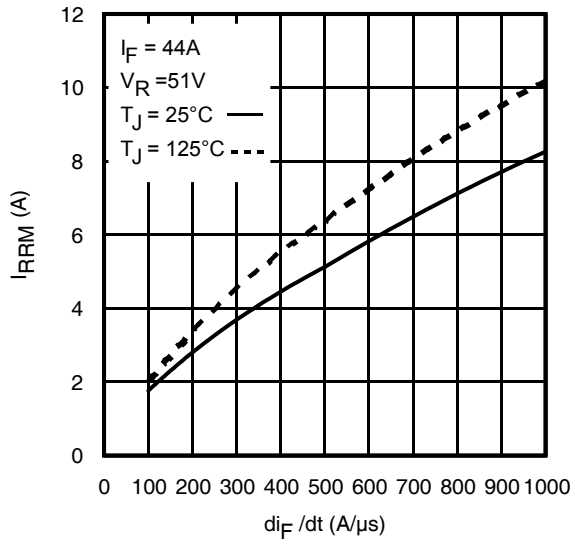


Fig 19. Typical Recovery Current vs. dif/dt

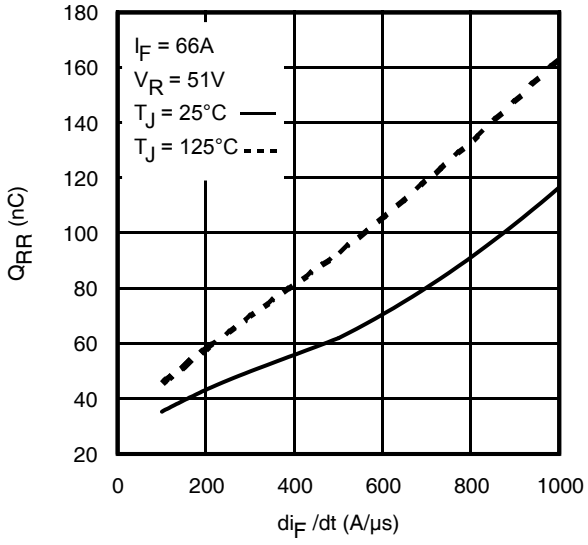


Fig 20. Typical Stored Charge vs. dif/dt

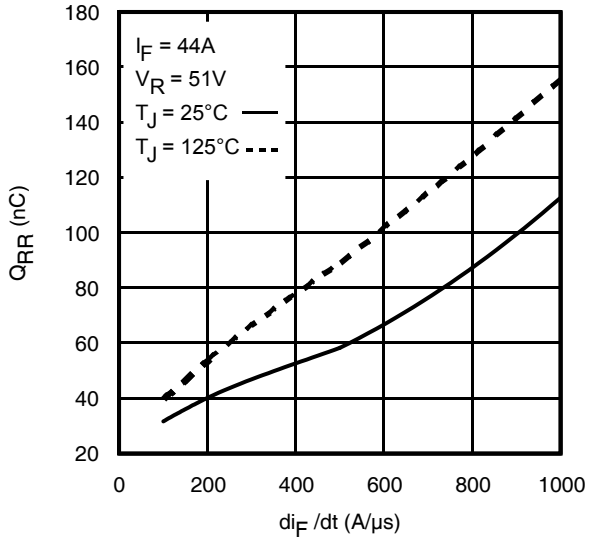


Fig 21. Typical Stored Charge vs. dif/dt